



The 20th IEEE International Conference on High Performance Computing and Communications (HPCC-2018)

28-30 June 2018, Exeter, UK

***** IEEE HPCC-2018 CFP *****

The 20th IEEE International Conference on High Performance Computing and Communications (HPCC-2018)

<http://cse.stfx.ca/~hpcc2018/>

Exeter, England, UK, 28-30 June 2018

Sponsored by

IEEE, IEEE Computer Society, and IEEE Technical Committee of Scalable Computing (TCSC)

INTRODUCTION

High Performance Computing and Communications has moved into the mainstream of computing and has become a key technology in determining future research and development activities in many academic and industrial branches. Among a series of highly successful International Conferences on High Performance Computing and Communications (HPCC), the HPCC-2018 conference is the 20th edition of a forum for engineers and scientists in academia, industry, and government to address the resulting profound challenges and to present and discuss their new ideas, research results, applications and experience on all aspects of high performance computing and communications.

HPCC-2018 will provide a high-profile, leading-edge forum for researchers, engineers, and practitioners to present state-of-art advances and innovations in theoretical foundations, systems, infrastructure, tools, testbeds, and applications for the HPCC, as well as to identify emerging research topics and define the future.

HPCC-2018 will be hosted in Exeter, the capital city of Devon and provides the county with a central base for education, medicine, religion, commerce and culture. The city is also home to the magnificent Exeter Cathedral, which dates back to Norman times. Exeter is also ideally placed to base a trip to branch out visiting places such as the famous Dartmoor National Park and the unspoilt beaches of the North and South Devon coastlines.

SCOPE AND TOPICS

Topics of interest include, but are not limited to:

Track 1: High Performance Computing and Applications

- High performance computing theory
- High performance computing architectures
- Parallel programming paradigms, models and languages
- Parallel algorithms
- Domain-specific parallel and distributed algorithms
- System software and middleware
- System software support for scientific workflows
- Storage and I/O systems
- Resource management
- Job scheduling

- Fault tolerance and resilience
- Exascale systems
- Instruction-level and thread-level parallelism
- Performance modeling and evaluation
- Languages and compilers for high performance computing
- Quantum computing
- Massively multicore systems
- Future novel computing platforms
- Database applications and data mining
- High performance computing for bioinformatics
- High performance computing for big data analytics
- High performance computing for data mining
- High performance computing for artificial intelligence
- High performance computing for block chains
- Green (power efficient) high performance computing

Track 2: Parallel and Distributed Computing and Systems

- Parallel and distributed system architectures
- Parallel and distributed software technologies
- Parallel and distributed algorithms
- Data center architectures
- Resource virtualization
- Web services and Internet computing
- Cloud computing
- Utility computing
- Grid and cluster computing
- Peer-to-peer computing
- Biological/molecular computing
- Resource management for parallel and distributed systems
- Embedded systems
- Distributed systems and applications
- Collaborative and cooperative environments
- Pervasive/ubiquitous computing and intelligence
- Tools and environments for parallel and distributed computing
- MapReduce, Hadoop, Spark, scalable computing and storage platforms
- Distributed Graphics and VR/AR/MR Systems
- Distributed AI and Soft/Natural Computing
- Power-efficient and green computing systems
- Parallel and distributed computing for big data
- Parallel and distributed computing for data mining
- Parallel and distributed computing for artificial intelligence

Track 3: Communications and Networking

- Network and interconnect architectures
- Communications and synchronization on parallel and distributed systems
- Mobile computing and wireless communications
- Computer Networks
- Internet architectures and protocols
- Telecommunications
- Autonomic computing, reliability, and fault-tolerance
- Trust, security, and privacy
- Energy-aware computing and networking

- 5G networks
- Software defined networking
- network functions virtualization
- Machine learning and deep learning
- Social networking and computing
- Performance evaluation and measurement

IMPORTANT DATES

- Workshop Proposal Due: 10 January 2018
- Paper Submission Deadline: ~~10 February 2018~~ 23 March 2018 (firm deadline)
- Authors Notification: 22 April 2018
- Camera-Ready Paper Due: 25 May 2018
- Early Registration Due: 25 May 2018
- Conference Date: 28-30 June 2018

PAPER SUBMISSION GUIDELINE

All papers need to be submitted electronically through the conference submission website (<http://cse.stfx.ca/~hpcc2018/sub/>) with PDF format. The materials presented in the papers should not be published or under submission elsewhere. Each paper is limited to 8 pages (or 10 pages with over length charge) including figures and references using IEEE Computer Society Proceedings Manuscripts style (two columns, single-spaced, 10 fonts). You can confirm the IEEE Computer Society Proceedings Author Guidelines at the following web page:

<http://www.computer.org/web/cs-cps/>

Manuscript Templates for Conference Proceedings can be found at:

https://www.ieee.org/conferences_events/conferences/publishing/templates.html

Once accepted, the paper will be included into the IEEE conference proceedings published by IEEE Computer Society Press (indexed by EI). At least one of the authors of any accepted paper is requested to register the paper at the conference.